USN | | | | | | | | | | |

10EC021

M.Tech. Degree Examination, December 2011
CMOS VLSI Design

Time: 3 hrs. Max. Marks:100

Note: ***1. Answer any FIVE full questions.***
2. Assume suitable missing data, if any.
3. Draw neat diagrams, wherever necessary.

1 a. With a neat diagram, explain the behaviour of nMOS enhancement mode MOSFET in different regions and draw the VI characteristics. **(10 Marks)**

b. Explain the following :
i) Channel length modulation.
ii) Threshold voltage – body effect. **(10 Marks)**

2 a. For a CMOS inverter, calculate the shift in the transfer characteristic when β_n/β_p ratios are 0.1, 1, 5 and draw the transfer characteristic with β ratio (use typical values). **(08 Marks)**

b. Explain the working of a BiCMOS inverter using MOS transistors and resistors and draw the input output characteristics. **(06 Marks)**

c. Explain the operation of a Pseudo – nMOS inverter and draw DC transfer characteristics. **(06 Marks)**

3 a. Using λ - based design rules, draw the layout for a nMOS 3 input NOR gate, using the following transistor Liw ratios.
i) p.u. transistor = 8:1
ii) p.d. transistors = 1:2, 1:2, 1:2.
Place the output point on the polysilicon layer. **(12 Marks)**

b. Calculate CMOS inverter pair delays interms of T, for the following diagram : **(08 Marks)**

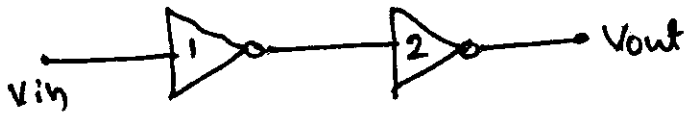

Fig.Q.3(b)

4 a. Draw the schematic and layout for given CMOS logic function $A = \overline{X.Y + W.Z}$. **(06 Marks)**

b. Design and implement 2:1 MUX based 8:1 MUX using transmission gates. **(08 Marks)**

c. Using the minimum number of transistors, draw the schematic diagram for a given CMOS logic function $Z = \overline{ABC + BCD + BE}$. **(06 Marks)**

5 a. An off chip capacitance load of 5pf is to be driven from nMOS inverters. Set out suitable arrangements giving appropriate channel Liw ratios. Calculate the number of inverter stages required, the width factor, input capacitance of each inverter and delay exhibited by the overall arrangement. Use the 5µm technology. **(10 Marks)**

b. Determine the node voltages V_1, V_2, V_3, V_4 and V_5 for the following pass transistor diagram where $V_{DD} = 5V$ and $V_{tn} = 1.5V$. **(05 Marks)**

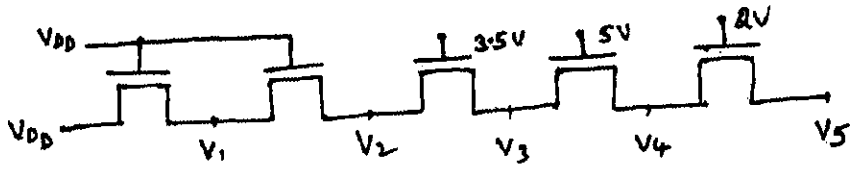

Fig.Q.5(b)

c. Derive the scaling factors of the following MOS parameters :
i) Gate delay – T_d ; ii) Gage capacitance – C_g. **(05 Marks)**

6 a. What is voltage bootstrapping? Explain the dynamic techniques, using transmission gates and dynamic CMOS logic. **(10 Marks)**

b. Explain the operation of clocked NOR based SR latch and JK latch. **(10 Marks)**

7 a. What is latch up? Explain the effect of latch up in p – well CMOS inverter structure. **(10 Marks)**

b. Explain the operation of domino CMOS structure. **(05 Marks)**

c. Analyze a nMOS current mirror circuit. **(05 Marks)**

8 a. Explain accumulation, depletion and channel inversion in an enhancement mode nMOS transistor. **(08 Marks)**

b. What is scaling? List the advantages of scaling. **(04 Marks)**

c. Explain the operation of a differential amplifier. **(08 Marks)**

* * * * *